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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,603	01/16/2001	Joerg Drescher	225/49512	9440

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EXAMINER	
STEVENS, THOMAS H	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/759,603	DRESCHER ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/20/2006 & 02/17/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7-11 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-11 and 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 7-11, 13-20 were examined.

2. Claims 4-6, and 12 were cancelled.

Section I: Non-Final Rejection (4th Non-Final)

Claim Objection

3. Claim 2 is objected to for a minor typo (2nd last line): "...to provide generation of logic circuits". Suggestion: "...to provide a generation of logic circuits..."

4. Claim 8 is objected to for a grammatical error (2nd line): "...of said drive module is provides signals required...". Appropriate action is requested.

Claim Rejections - 35 USC § 103

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1, 2,3,7,8, 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bentley (US Patent 4,075,677) in view of Spizter et al., "Interface Technologies for Versatile Rapid-Prototyping Systems" June 1999 (hereafter Spizter). Bentley and Spizter are analogous art because they both teach electronic circuits.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the circuit simulation of Spizter in the regulation/control circuits of Bentley because Spizter teaches a method in which no time-consuming development of additional interfaces has to be done. This will save up to several days if previous versions of the control unit are available and have only to be modified. This saved time gives a competitive edge in the development process (Spitzer: pg. 209, Summary section, 2nd paragraph).

Claim 1. An apparatus for simulating (Spitzer: figure 1) an electrical sensor/actuator (Spitzer: pg. 204, right column, 2nd paragraph) component, comprising: a drive module (Spitzer: pg.208, right column, figure 12) including a model of the sensor/actuator (Spitzer: pg. 204, right column, 2nd paragraph) component, said drive module (Spitzer: pg.208, right column, figure 12) generating interface signals (Spitzer: pg.206, left column 3rd paragraph) in accordance with signals of said sensor/actuator (Spitzer: pg.208, right column, figure 12) component being simulated, (Spitzer: figure 1) said drive module (Spitzer: pg.208, right column, figure 12) further including at least one signal interface (Spitzer: pg.206, left column 3rd paragraph) with each one of said at least one signal interface (Spitzer: pg.206, left column 3rd paragraph) including and output stage with a four quadrant (Spitzer: pg.209, left column 1st sentence) which functions to one of receiver or output power (Spitzer: pg. 207, left column, lines 3-4) and with each of said at least one signal interfaces (Spitzer: pg.206, left column 3rd paragraph) being associated with a respective connection pin (Bentley: column 12, line 44) which is driven by real-time (Spitzer: pg.205, left column 1st sentence) signals from said drive module (Spitzer: pg.208, right column, figure 12) and wherein said at least one signal interface (Spitzer: pg.206, left column 3rd paragraph) generates, for each said interface connection pin (Bentley: column 12, line 44), one of said interface signals (Spitzer: pg.206, left column 3rd paragraph) corresponding to the electrical signals of said sensor/actuator component; wherein each of said at least one signal interface (Spitzer: pg.206, left column 3rd paragraph) includes a control/regulation circuit (Bentley: column 16, lines 46 and 54-55) for directing current or energy of said

generated interface signals (Spitzer: pg.206, left column 3rd paragraph) in a direction either towards said at least one signal interface (Spitzer: pg.206, left column, 3rd paragraph) or away (bi-directional, Spitzer: pg. 206, left column, 3rd paragraph, bullet 1) from said at least one signal interface (Spitzer: pg.206, left column 3rd paragraph) whereby a sensor or an actuator can be optionally simulated (Spitzer: pg. 205, section 2.4).

Claim 2. An apparatus for simulating an electrical sensor/actuator (Spitzer: pg. 204, right column, 2nd paragraph) component, comprising: a drive module (Spitzer: pg.208, right column, figure 12) including a model of the sensor actuator component, said drive module (Spitzer: pg.208, right column, figure 12) generating interface signals (Spitzer: pg.206, left column 3rd paragraph) in accordance with signals of said sensor/actuator component being simulated, (Spitzer: pg. 205, section 2.4) said drive module (Spitzer: pg.208, right column, figure 12) further including a plurality of signal interfaces (Spitzer: pg.206, left column 3rd paragraph) with each of said being associated with a respective connection pin (Bentley: column 12, line 44) which is driven by a real-time (Spitzer: pg.205, left column 1st sentence) signals said drive module (Spitzer: pg.208, right column, figure 12) and wherein said plurality of signal interfaces (Spitzer: pg.206, left column 3rd paragraph) generates, for each said interface connection pin (Bentley: column 12, line 44), one of said an interface signals (Spitzer: pg.206, left column 3rd paragraph) corresponding to the electrical signals (Spitzer: 205, section 2.2, line 6) of said sensor/actuator component; a main printed board (Spitzer: 205, section 2.2, line 5)

having one insertion location for each interface connection for each of said interface pins (Bentley: column 12, line 44) and wherein one of said signal interfaces (Spitzer: pg.206, left column 3rd paragraph) is provided for each location; wherein said apparatus includes modular construction in order to provide a separate signal interface (Spitzer: pg.206, left column 3rd paragraph) for each interface component and wherein each of said plurality of signal interfaces (Spitzer: pg.206, left column 3rd paragraph) are essentially the same to provide generation of logic signals (a plurality of signals with different power levels, etc. Spitzer: pg. 206, paragraphs 3-4) for a data line.

Claim 3. The apparatus according to Claim 1, wherein said drive module (Spitzer: pg.208, right column, figure 12) further includes means for calculating mathematical modules for driving said at least one signal interface (Spitzer: pg.206, left column 3rd paragraph) and wherein said module generates said real-time (Spitzer: pg.205, left column 1st sentence) signals in order to obtain said interface signals (Spitzer: pg.206, left column 3rd paragraph) in accordance with the simulated (Spitzer: pg. 205, section 2.4) sensor/actuator components at the interface connection pins (Bentley: column 12, line 44).

Claim 7. The apparatus according to Claim wherein said drive module (Spitzer: pg.208, right column, figure 12) comprises a computer for providing an equivalent circuit (Inherent: well-known within the art of circuit design) of the sensor/actuator component as said model.

Claim 8. The apparatus according to Claim 1, wherein said model of said drive module (Spitzer: pg.208, right column, figure 12) is provides signals required at an interface connection pin (Bentley: column 12, line 44) by utilizing specific parameters.

Claim 13. The apparatus according to Claim 2, wherein said drive module (Spitzer: pg.208, right column, figure 12) further includes means for calculating mathematical (Spitzer: pg. 205, section 2.4, 1st paragraph, "MathWorks") modules for driving said at least one signal interface (Spitzer: pg.206, left column 3rd paragraph) and wherein said module (Spitzer: pg. 205, section 2.5) generates said real-time (Spitzer: pg.205, left column 1st sentence) signals in order to obtain said interface signals (Spitzer: pg.206, left column 3rd paragraph) in accordance with the simulated (Spitzer: pg. 205, section 2.4) sensor/actuator components at the interface (Spitzer: pg. 205, 1st paragraph) connection pins (Bentley: column 12, line 44).

Claim 14. The apparatus according to Claim 2, further including a main printed circuit board having one insertion location for each interface connection (Spitzer: pg. 205, 1st paragraph) for each of said interface pins (Bentley: column 12, line 44) and wherein one of said signal interfaces (Spitzer: pg.206, left column 3rd paragraph) is provided for each insertion location.

Claim 15. The apparatus according to Claim 2, wherein each of said signal interfaces (Spitzer: pg. 206, left column 3rd paragraph) has an output stage (Spitzer: pg. 206, last paragraph "output modules").

Claim 16. The apparatus according to Claim 2, wherein said output stage is a four-quadrant amplifier (Spitzer: pg. 204 figure 1 "Sensor Amplifier" and pg. 209, left column, line 1 "real four-quadrant operation"), which can function to output power (Spitzer: pg. 207, left column, line 6) or to receive power.

Claim 17. The apparatus according to Claim 2, wherein said drive module (Spitzer: pg. 208, right column, figure 12) comprises a computer for prodding an equivalent circuit (Inherent: well-known within the art of circuit design) of the sensor/actuator component as said model.

Claim 18. The apparatus according to Claim 2, wherein said model of said drive module (Spitzer: pg.208, right column, figure 12) is adapted to signals required (Spitzer: pg. 205, section 2.5, 4th paragraph, lines 9-10) at an interface (Spitzer: pg. 205, 1st paragraph) connection pin (Bentley: column 12, line 44) by utilizing specific parameters.

Claim 19. The apparatus according to Claim 2, further comprising a fault simulation module (Spitzer: pg. 205, section 2.5) for generating one of a line interruption (Spitzer: pg. 206, right column, 1st paragraph, line 5) and a short circuit (Ohm's Law).

Claim 20. The apparatus according to Claim 2, wherein each of said signal interfaces (Spitzer: pg.206, left column 3rd paragraph) has a regulating circuit (Bentley: column 16, line 54) for adjusting (Bentley: column 5, lines 4-7) one of voltage and current to a value specified by said model.

8. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bentley (US Patent 4,075,677) in view of Spizter as applied to claim 1, and further in veiw of Goel (US Patent 4,204,633).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine Goel with Bentley and Spizter because, Goel teaches a method that is faster by more than an order of magnitude for error correction and detection type logic and is simpler and therefore less expensive to implement (Goel: column 3, lines 60-65). Spizter teaches a method in which no time-consuming development of additional interfaces has to be done. This will save up to several days if previous versions of the control unit are available and have only to be modified.

Claim 9. The apparatus according to Claim 1, further comprising a fault simulation (Goel: column 5, lines 1-2) module for generating one of a line interruption (Spitzer: pg. 206, right column, 1st paragraph, line 5) and a short circuit (Ohm's Law).

Claim 10. The apparatus according to Claim 1, wherein each of said signal interfaces (Spitzer: pg.206, left column 3rd paragraph) has a regulating circuit (Bentley: column 16, line 54) for adjusting (Bentley: column 5, lines 4-7) one of voltage and current to a value specified by said model.

Claim 11. The apparatus according to Claim 10, wherein said regulating circuit includes a feedback arrangement (Goel: column 2, line 66) to the drive module (Spitzer: pg.208, right column, figure 12) in order to provide actual values of regulated variables ("model variables" Spitzer: pg. 207, right column, last paragraph) to said model.

Section II: Response to Applicants' Arguments (3rd Office Action)

112 2nd

9. Applicants are thanked for addressing this issue. Rejection is withdrawn.

103(a)

10. Applicant's arguments, see pages 6-11, filed 01/20/2006, with respect to the rejection of claims 1-3,7-11 and 13-20 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Bentley, Goel and Spizter.

Drawings

11. The Office acknowledges the response (02/17/2006) to this issue. Objection is withdrawn.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Paul Rodriguez 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

April 25, 2006

TS

Paul L. Rodriguez 5/1/06
Primary Examiner
Art Unit 2125